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L1 2602 S VIRTUAL ADDRESS##
L2 4622 S PHYSICAL ADDRESS##
L3 889 S LINEAR ADDRESS##
L4 3969 S (ABSOLUTE OR ACTUAL) (2W) ADDRESS##
L5 48 S L1 AND L2 AND L3 AND L4
L6 5110 S SEGMENTATION
L7 6543 S PAGING
L8 200 S L6 (P) L7

=> s l8 and l5

L9 8 L8 AND L5

=> set high off

SET COMMAND COMPLETED

=> s l9;set high on;s l1 (8a) l3

L10 8 L8 AND L5

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Document Number 9

Entry 9 of 11

File: USPT

Nov 4, 1986

DOCUMENT-IDENTIFIER: US 4621320 A
TITLE: Multi-user read-ahead memory

BSPR:

Many sophisticated algorithms for prefetching data into a buffer, or cache, memory, some of which such algorithms adaptively prefetch along multiple lines, exist. A simplistic algorithm for loading a page, or block, of data words into the buffer memory when one of the data words is requested from the memory unit may be based upon the limited assumption that requests to such memory unit will tend to be somewhat sequential in nature, such sequential nature as results from the general flow of digital computer software programs. If the flow is generally sequential, then the next data word following that data word which has been requested from the memory system will be the most likely candidate for future accesses. As buffer, or cache, memories are increased in size and the number of data words which are prefetched into the buffer memory becomes larger, then the benefit of such prefetching, based on the likelihood that the next request will be a request for one of the cached data words, increases. But such increase is not in direct proportion to the number of data words being added to the buffer, regardless of the sophistication and the multiplicity of the prefetching algorithms (including the sequential algorithm).

BSPR:

Also in the Scheuneman invention, the very next subsequent reference to the asynchronous memory unit must be, in order to utilize the pre-fetched data word, a reference to the next sequential address. The present invention accords that data words will be prefetched for only one(s) of a multiplicity of requestors, and that intervening requests of other requestors subsequent to the prefetching will not disturb the prefetched data word. Thus the speed advantage of prefetching is maintained even when the next subsequent reference is not to that next sequential address for which data has been read ahead, or prefetched.

CCOR:711/213

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Document Number 10

Entry 10 of 11

File: USPT

DOCUMENT-IDENTIFIER: US 4370711 A

TITLE: Branch predictor using random access memory

BSPR:

This invention relates to the branch prediction mechanism for handling conditional branch instructions in a computer system. When a branch instruction is encountered, it is wasteful of the computer resource to wait for resolution of the instruction before proceeding with the next programming step. Therefore, it is a known advantage to provide a prediction mechanism to predict in advance the instruction to be taken as a result of the conditional branch. If this prediction is successful, it allows the computer system to function without a delay in processing time. There is a time penalty if the prediction is incorrect. Therefore, an object of the present invention is to provide an improved branch prediction mechanism with a high prediction accuracy to minimize the time loss caused by incorrect predictions.

CCXR:711/213

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